-- 10. A semiconductor integrated circuit according to claim 6, wherein said plurality of functional blocks includes a CPU core block.

11. A semiconductor integrated circuit according to claim 6, wherein said plurality of functional blocks includes a memory cell block.

12. A method of manufacturing a semiconductor integrated circuit comprising a plurality of functional blocks and a gate array block, each of said plurality of functional blocks being respectively completed by a layout design, the method comprising the steps of:

placing the gate array block, comprised of a plurality of basic cells arranged in line, within a first area of a semiconductor chip and said plurality of functional blocks within a second area of said semiconductor chip;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells lying within the gate array block by using interconnections in accordance with the designed circuits whereby said designed circuits are formed on said semiconductor chip. --

REMARKS

The Office Action dated September 25, 2000 has been received and its contents carefully considered. The disclosure has been editorially amended, Claims 1-9 amended and new claims 10-12 added to the application. Reconsideration and withdrawal of the outstanding rejections are respectfully requested in view of the foregoing amendments and the following remarks.

1. Paragraph 2 of the Office Action states "Claims 1 through 8 comply with the requirements of 35 U.S.C. 112." Since claim 9 was also in the application as originally filed, Applicants are unclear as to whether claim 9 is considered to comply with 35 U.S.C 112. In any event, claim 9 has been amended to ensure compliance with Section 112, and it is submitted that all of the claims now in the application fully comply with the statute.

2. In paragraph 3 of the Office Action, claims 1-7 and 9 are rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent 5,539,224 to Ema. This rejection if applied to the amended claims is respectfully traversed.

Ema teaches designing and forming a layout of two or more unit circuit-blocks on a common chip, each having a separate function, and interconnection between the unit circuit-blocks (col. 1, lines 16-20). The Action cites Fig. 7 of Ema as teaching an integrated circuit comprising a plurality of basic cell functional blocks. However, as shown clearly in Fig. 6 and col. 2, lines 48-59 of Ema, each of the unit circuit blocks is given a separate function by sequentially designing and exposing the blocks. Thus, Ema fails to disclose using fixed function blocks (function blocks with a predetermined function prior to placement on the chip) in combination with a gate array block (a block assigned a function only after the placements of both the functional and gate array blocks). Also in paragraph 3 the Action cites Fig. 9 of Ema for teaching interconnections. However, as shown in Figs. 5A and 9, Ema only discloses establishing electrical interconnections between the various unit circuit blocks; he does not teach connecting basic cells within a gate array block.

The present invention teaches a method in independent claim 1 and an apparatus in independent claim 6 whereby a plurality of functional blocks and a gate array block are

placed within a predetermined area of a semiconductor chip. The functional blocks are provided with predetermined functions by semiconductor devices. The gate array block is comprised of a plurality of basic cells that at this stage are not yet provided with any particular function. Thereafter, a circuit with the desired function is designed using the gate array block. In the next step, the basic cells within the gate array block are electrically connected to other basic cells using electrical interconnections in accordance with the circuits designed in the previous step.

An important element of independent claims 1 and 6 of the present invention is the use of the combination of a gate array block, which is assigned a function after fabrication, and functional blocks, which have a predetermined function. Ema fails to teach or suggest this aspect of the present invention. This difference is highly significant because the method of claim 1 can reduce the time to manufacture a completed integrated circuit by several months to several weeks as set forth at page 10, lines 25-29 of Applicants' disclosure. This method allows for both speed in manufacturing and the ability to customize according to individual customer demands.

Thus, amended independent claims 1 and 6, and amended claims 2-5 and 7- 9, which are dependent thereon, are considered patentable over the Ema reference.

3. In paragraph 4 of the Office Action, claims 2, 3, 4 and 9 are rejected under 35 U.S.C. 102 as being anticipated by Ema. Claims 2, 3 and 4 are dependent on claim 1, and claim 9 is dependent on claim 6. It is submitted that claims 2, 3, 4 and 9 are allowable over Ema for the reasons given above for the allowability of claim 1.

4. In paragraph 5 of the Office Action, claim 7 is rejected under 35 U.S.C. 102 as being anticipated by Ema. It is submitted that claim 7, dependent on claim 6, is allowable over Ema for the reasons given above for the allowability of claim 6

5. In paragraph 6 of the Office Action, claim 8 is rejected under 35 U.S.C. 103 as being unpatentable over Ema and U.S. Patent 4,766,475 to Kawashima. Kawashima teaches a semiconductor integrated circuit, including a technique for increasing the density of integration of input and output buffers in the semiconductor integrated circuit (col. 1, lines 10-17 in Kawashima). Kawashima neither teaches nor suggests a semiconductor integrated circuit having a gate array block with a circuit designed after placement of both the functional blocks and the gate array blocks. Accordingly, Applicants' submit that claim 8 is patentable because Kawashima does not supply the elements missing from Ema, and because it depends from independent claim 6 which is considered allowable for the reasons given above for the patentability of claims 1-7 and 9.

It is submitted that the present application is in condition for allowance, and allowance thereof with claim 1-12 is requested.

Respectfully submitted,

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